**Сводный отчет использования ресурсов микросхемы Spartan3E при моделировании нейросети Джордана**

**Дискретная модель сети Джордана (4 входа, 8 нейронов, 9 бит/коэффициент)**

Design Statistics

# IOs : 443

Cell Usage :

# BELS : 2482

# GND : 1

# LUT2 : 44

# LUT2\_L : 7

# LUT3 : 405

# LUT4 : 583

# LUT4\_L : 4

# MULT\_AND : 64

# MUXCY : 640

# MUXF5 : 13

# VCC : 1

# XORCY : 720

# FlipFlops/Latches : 13

# FD : 2

# FDE : 8

# FDRS : 1

# FDS : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 442

# IBUF : 437

# OBUF : 5

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Device utilization summary:

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Selected Device : 3s500eft256-5

Number of Slices: 582

Number of Slice Flip Flops: 13

Number of 4 input LUTs: 1043

Number of IOs: 443

Number of bonded IOBs: 443

Number of GCLKs: 1

Minimum period: 33.457ns (Maximum Frequency: 29.889MHz)

Minimum input arrival time before clock: 33.467ns

Maximum output required time after clock: 36.738ns

Maximum combinational path delay: 36.748ns

**Непрерывная модель сети Джордана (4 входа, 8 нейронов, 32 бит/коэффициент)**

Design Statistics

# IOs : 1547

Cell Usage :

# BELS : 9243

# GND : 1

# INV : 7

# LUT2 : 42

# LUT3 : 1751

# LUT4 : 2081

# LUT4\_D : 1

# MULT\_AND : 248

# MUXCY : 2551

# VCC : 1

# XORCY : 2560

# FlipFlops/Latches : 16

# FD : 2

# FDE : 11

# FDRS : 1

# FDS : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 1546

# IBUF : 1541

# OBUF : 5

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Device utilization summary:

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Selected Device : 3s500eft256-5

Number of Slices: 2034

Number of Slice Flip Flops: 16

Number of 4 input LUTs: 3882

Number of IOs: 1547

Number of bonded IOBs: 1547

Number of GCLKs: 1

Minimum period: 38.203ns (Maximum Frequency: 26.176MHz)

Minimum input arrival time before clock: 38.282ns

Maximum output required time after clock: 41.104ns

Maximum combinational path delay: 41.183ns